Integrated Circuit Design

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Text Book (2/2)
Prof. Weste’s Brief Biography

- Neil Weste has a BSc, BE(Elec.) and PhD from the University of Adelaide. He spent 18 years in the US working for Bell Labs, MCNC and Symbolics Inc. before co-founding TLW Inc., an IC design house in Burlington, MA. He commenced working for Bell Labs in 1977 working on early VLSI design tools (the MULGA suite). He was VP Design&Systems at MCNC in North Carolina. In 1984 he joined Symbolics to lead an effort on the Ivory single chip Lisp machine. He returned to Australia in 1995 as Professor of Microelectronic Systems at Macquarie University. In 1997, he co-founded Radiata Communications, which pioneered single chip implementations of the IEEE 802.11a Wireless LAN standard. In 2004, he founded NHEW R&D Pty Ltd, which manages angel investments in Australian high technology companies and carries out R&D in the RF IC area.

- Dr Weste is co-author of a best selling text on CMOS IC design originally published in 1985 and now in its third edition (May 2004). He is a Fellow of the IEEE and is a peer elected member of the IEEE Solid State Circuits administrative committee. He is an adjunct professor at Macquarie University and the University of Adelaide.
Course Goal

- Introduce the **fundamental concepts and advanced techniques** for the VLSI and SOC system design
- Introduce the **basic and necessary tools** used in the VLSI-SOC system design
- Undergraduate students for one semester
Course Impact (1/2)

VLSI and SOC Design

- VLSI Digital Signal Processing System Design
- Digital Signal Processor Design
- 3D Graphics Systems
- Computer Architecture
- Multimedia-Communications System-on-Chip Design
- Biomedical Circuits and Systems
Course Impact (2/2)

- 雲端雙星
  - 半導體產業
  - 影像顯示產業
- 生物技術與醫藥工業
- 數位內容產業

精神：傳統以成本為競爭核心的大規模製造方式，已無法創造長久的競爭優勢。新經濟的競爭力來自創新、應用知識的能力及效率。

Lan-Da Van

VLSI and SOC Design
Course Value

**Cluster Theory (群聚效應)**

- 施敏教授說: 在人類社會歷史中，很多文明歷史是非常集中的！
- 唐詩的發展集中於西元700~850年間。
  - 代表人: 李白、杜甫、白居易。
- 古典音樂的盛世是在西元1700~1850年間。
  - 代表人: 莫札特、貝多芬、蕭邦。
- 理論與實驗物理是在西元1880~1980年間。
  - 代表人: 愛因斯坦。
- 電子資訊的世代則是在西元1950~2050甚至2100年因此大家要有信心，未來的100年仍是電子與資訊的天下！

摘自交大友聲426期, pp. 66-71.
Syllabus (1/2)

- Lecture 1 Welcome to VLSI
  - VLSI/SOC IC History, VLSI/SOC

- Lecture 2 Devices
  - CMOS Process Technology, Circuit Characterization and Performance Estimation

- Lecture 3 Speed
  - Logical Effort, Delay Calculation, Power Dissipation

- Lecture 4 Power
  - Dynamic Power, Static Power, Energy-Delay Optimization, Low Power Architecture

- Lecture 5 Wire
  - Interconnect Modeling, Interconnect Impact

- Lecture 6 Scaling and Reliability
  - Scaling, Reliability

- Lecture 7 SPICE
  - SPICE command, Device Model, Device Characteristics, Circuit Characteristics
Syllabus (2/2)

- **Lecture 8 Gates**
  - Static Circuits, Dynamic Circuits, Transmission Gate, Skew Gate, Delay Calculation

- **Lecture 9 Sequencing**
  - Latch and Flip-Flop, State Assignment, Power Analysis

- **Lecture 10 Datapaths**
  - Shifter, Adder, Multiplier, ALU

- **Lecture 11 Memories**
  - SRAM, DRAM, ROM and Its Variations

- **Lecture 12 Methodology**
  - Front-end Design and Analysis Tool
  - Platform-based SOC design
授課方式 & 評分標準

教授授課

評分標準

- 期中考：30%
- 期末考：40%
- Lab：20%
- 作業/Quiz: 10%
- 出席: 0.25N%（表示全學期點名共N次，每次點名均出席加0.25N分，一次曠課加0.25(N-1)分，兩次曠課加0.25(N-2)分，...,”施主”均沒有出席則不加分）

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總和: (100+0.25N)%

Material Web-Site:

- http://viplab.cs.nctu.edu.tw/course/VLSI_SOC2013_Fall.htm

Teaching Assistant:

- 吳宗翰 (e-mail: zong-han@viplab.cs.nctu.edu.tw ; 分機: 59283)
Homework is not “Teamwork”!!
You can discuss with each other but not “COPY”!!
Don’t miss hard deadline for each homework!!