Welcome to VLSI

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Integrated Circuits (IC) – imply to pack many components in a circuit.

- **Small Scale Integration (SSI)** in 1970s – A couple of gates or a flip flop.
- **Large Scale Integration (LSI)** in 1980s – Functional unit and memory with low computation power and capability.
- **Very Large Scale Integration (VLSI)** in 1990s – millions of transistors (electrical switching device).
- **System-on-a-Chip (SOC)** in 2000s
The First Computer

- The Babbage Difference Engine (1832)
- Mechanical parts: 25,000
- Cost: 17,470 (pound)

ENIAC - The First Electronic Computer (1946, 1/3)

- Vacuum Tube #: 17,468
- Resistors: 70,000
- Capacitor: 10,000
- Manual Switches: 6,000
- Size:
  - 80 feet long
  - 30 feet wide
  - 8.5 feet high

ENIAC - The First Electronic Computer (1946, 2/3)

- ENIAC (Electrical Numerical Integrator And Calculator, 電子數字積分計算機)
- 5000 addition per second OR 400 multiplications per second (200,000 times speed up compared with hand calculation)
- 17,468 vacuum tubes
- 70,000 resistors
- 10,000 capacitors
- 1,500 relays
- 6,000 manual switches
- 160 kilowatts
- 167 square meters
- 30 tons
ENIAC - The First Electronic Computer (1946, 3/3)

- ENIAC filled an entire room!
- Could add 5,000 numbers in a single second?
- Debug?
In 1947, Grace Murray Hopper was working on the Harvard University Mark II Aiken Relay Calculator (a primitive computer).

On the 9th of September, 1947, when the machine was experiencing problems, an investigation showed that there was a moth trapped between the points of Relay #70, in Panel F.

First actual case of bug being found.
The First Transistor (1947)

- First transistor invented at Bell Labs, 1947.
- Dr. Bardeen, Shockley, Brattain were awarded the Nobel prize in 1956!

The First Integrated Circuit (IC) (1958)

- Dr. Jack Kilby at TI
- Passive and Active are integrated on a single semiconductor substrate
- Dr. Robert Noyce (1959) proposed the similar idea at the same time. So, patent issue?
- Dr. Jack Kilby was awarded the Nobel prize at 2000! (Why?)

**The First Logic IC’s (1961)**

**1961:** TI and Fairchild introduced the first logic IC’s (cost ~$50 in quantity!). This is a dual flip-flop with 4 transistors.

**1963:** Densities and yields are improving. This circuit has four flip flops.

**1967:** Fairchild markets the semi-custom chip shown below. Transistors could be easily rewired using a two-layer interconnect to create different circuits. This circuit contains ~150 logic gates.

**1968:** Intel成立

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Source: Marcel Jacomet
INTegrated ELectronics=Intel (1968)

Noyce and Moore leave Fairchild and found Intel. No business plan, just a promise to specialize in memory chips. They and Art Rock raise $2.5M in two days and move to Santa Clara. By 1971 Intel had 500 employees; by 1983 it had 21,500 employees and $1.1B in sales.

Pioneers of the Electronic Age
In 1970, making good on its promise to its investors Intel (Joel Karp, Les Vadasz, John Reed) starts selling a 1K bit PMOS RAM. It was a bear to interface to, but its density and cost make it the only game in town. Core memory dies…
Intel 4004 Micro-Processor (1971)

- First microprocessor (1971)
  - For Busicom calculator

- Characteristics
  - 10 μm process
  - 2300 transistors
  - 400 – 800 kHz
  - 4-bit word size
  - 16-pin DIP package

- Masks hand cut from Rubylith
  - Drawn with color pencils
  - 1 metal, 1 poly (jumpers)
  - Diagonal lines (!)
8008

- 8-bit follow-on (1972)
  - Dumb terminals

- Characteristics
  - 10 μm process
  - 3500 transistors
  - 500 – 800 kHz
  - 8-bit word size
  - 18-pin DIP package

- Note 8-bit datapaths
  - Individual transistors visible
16-bit address bus (1974)
- Used in Altair computer
  - (early hobbyist PC)

Characteristics
- 6 µm process
- 4500 transistors
- 2 MHz
- 8-bit word size
- 40-pin DIP package
8086 / 8088

- 16-bit processor (1978-9)
  - IBM PC and PC XT
  - Revolutionary products
  - Introduced x86 ISA

Characteristics
- 3 μm process
- 29k transistors
- 5-10 MHz
- 16-bit word size
- 40-pin DIP package

Microcode ROM
Virtual memory (1982)
- IBM PC AT

Characteristics
- 1.5 μm process
- 134k transistors
- 6-12 MHz
- 16-bit word size
- 68-pin PGA

Regular datapaths and ROMs

Bitslices clearly visible
80386

- 32-bit processor (1985)
  - Modern x86 ISA
- Characteristics
  - 1.5-1 μm process
  - 275k transistors
  - 16-33 MHz
  - 32-bit word size
  - 100-pin PGA
- 32-bit datapath, microcode ROM, synthesized control
Pipelining (1989)
- Floating point unit
- 8 KB cache

Characteristics
- 1-0.6 μm process
- 1.2M transistors
- 25-100 MHz
- 32-bit word size
- 168-pin PGA

Cache, Integer datapath, FPU, microcode, synthesized control
Pentium

- Superscalar (1993)
  - 2 instructions per cycle
  - Separate 8KB I$ & D$
- Characteristics
  - 0.8-0.35 μm process
  - 3.2M transistors
  - 60-300 MHz
  - 32-bit word size
  - 296-pin PGA
- Caches, datapath, FPU, control
Pentium Pro / II / III

- Dynamic execution (1995-9)
  - 3 micro-ops / cycle
  - Out of order execution
  - 16-32 KB I$ & D$
  - Multimedia instructions
  - PIII adds 256+ KB L2$

- Characteristics
  - 0.6-0.18 μm process
  - 5.5M-28M transistors
  - 166-1000 MHz
  - 32-bit word size
  - MCM / SECC
Pentium 4

- Deep pipeline (2001)
  - Very fast clock
  - 256-1024 KB L2$

- Characteristics
  - 180 – 90 nm process
  - 42-125M transistors
  - 1.4-3.4 GHz
  - 32-bit word size
  - 478-pin PGA

- Units start to become invisible on this scale
The Dies of Intel CPUs

Pentium Pro

386

4004
## Semiconductor Technology Roadmap

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology node (nm)</td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
</tr>
<tr>
<td>On-chip local clock (GHz)</td>
<td>0.75</td>
<td>1.25</td>
<td>2.1</td>
<td>3.5</td>
<td>6.0</td>
<td>10</td>
<td>16.9</td>
</tr>
<tr>
<td>Microprocessor chip size (mm²)</td>
<td>300</td>
<td>340</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
<td>901</td>
</tr>
<tr>
<td>Microprocessor transistor/chip</td>
<td>11M</td>
<td>21M</td>
<td>76M</td>
<td>200M</td>
<td>520M</td>
<td>1.40B</td>
<td>3.62B</td>
</tr>
<tr>
<td>Microprocessor cost/transistor (x10⁻⁸ USD)</td>
<td>3000</td>
<td>1735</td>
<td>580</td>
<td>255</td>
<td>110</td>
<td>49</td>
<td>22</td>
</tr>
<tr>
<td>DRAM bits per chip</td>
<td>256M</td>
<td>1G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
<td>1T</td>
</tr>
<tr>
<td>Wiring level</td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.8-2.5</td>
<td>1.5-1.8</td>
<td>1.2-1.5</td>
<td>0.9-1.2</td>
<td><strong>0.6-0.9</strong></td>
<td>0.5-0.6</td>
<td>0.37-0.42</td>
</tr>
<tr>
<td>Power (W)</td>
<td>70</td>
<td>90</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
<td>183</td>
</tr>
</tbody>
</table>

Source: SIA99
Summary

$10^4$ increase in transistor count, clock frequency over 30 years!

<table>
<thead>
<tr>
<th>Processor</th>
<th>Year</th>
<th>Feature Size (μm)</th>
<th>Transistors</th>
<th>Frequency (MHz)</th>
<th>Word size</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>4004</td>
<td>1971</td>
<td>10</td>
<td>2.3k</td>
<td>0.75</td>
<td>4</td>
<td>16-pin DIP</td>
</tr>
<tr>
<td>8008</td>
<td>1972</td>
<td>10</td>
<td>3.5k</td>
<td>0.5–0.8</td>
<td>8</td>
<td>18-pin DIP</td>
</tr>
<tr>
<td>8080</td>
<td>1974</td>
<td>6</td>
<td>6k</td>
<td>2</td>
<td>8</td>
<td>40-pin DIP</td>
</tr>
<tr>
<td>8086</td>
<td>1978</td>
<td>3</td>
<td>29k</td>
<td>5–10</td>
<td>16</td>
<td>40-pin DIP</td>
</tr>
<tr>
<td>80286</td>
<td>1982</td>
<td>1.5</td>
<td>134k</td>
<td>6–12</td>
<td>16</td>
<td>68-pin PGA</td>
</tr>
<tr>
<td>Intel386</td>
<td>1985</td>
<td>1.5–1.0</td>
<td>275k</td>
<td>16–25</td>
<td>32</td>
<td>100-pin PGA</td>
</tr>
<tr>
<td>Intel486</td>
<td>1989</td>
<td>1–0.6</td>
<td>1.2M</td>
<td>25–100</td>
<td>32</td>
<td>168-pin PGA</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993</td>
<td>0.8–0.35</td>
<td>3.2–4.5M</td>
<td>60–300</td>
<td>32</td>
<td>296-pin PGA</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>1995</td>
<td>0.6–0.35</td>
<td>5.5M</td>
<td>166–200</td>
<td>32</td>
<td>387-pin MCM PGA</td>
</tr>
<tr>
<td>Pentium II</td>
<td>1997</td>
<td>0.35–0.25</td>
<td>7.5M</td>
<td>233–450</td>
<td>32</td>
<td>242-pin SECC</td>
</tr>
<tr>
<td>Pentium III</td>
<td>1999</td>
<td>0.25–0.18</td>
<td>9.5–28M</td>
<td>450–1000</td>
<td>32</td>
<td>330-pin SECC2</td>
</tr>
<tr>
<td>Pentium 4</td>
<td>2001</td>
<td>0.18–0.13</td>
<td>42–55M</td>
<td>1400–3200</td>
<td>32</td>
<td>478-pin PGA</td>
</tr>
</tbody>
</table>
Moore’s Law

Predicted that the number of transistors per chip would grow exponentially (double every 18 months).

Electronics, April 19, 1965.
Productivity Gap

Evolution of Silicon Technology

- First bipolar Transistor (1947)
- First MOSFET (1960)
- One-transistor DRAM cell Invented (1968)
- CMOS Invented (1963)
- IC Invented (1958)
- First Microprocessor (1971)

- Computer Focus
- Comm./Consumer Focus
- PC μp + Memory
- Mobile Wireless DSP + Analog

- Heterogeneous
- IP and Platform-based Design
- Scalable, reuse methodology

Lecture 1

Lan-Da Van
Integrated Circuits Overview

Analog Circuits
- AD Converter
- RF Circuit

Digital Circuits
- Control Logic
- ALU
- Memory Unit

Lecture 1
Introduction to VLSI and System-on-Chip Design
What is System-on-a-Chip?

**Definition**: integration of a complete system onto a single IC.

**Benefits of SoC**
- Reduce overall system cost
- Increase performance
- Low power consumption
SoC Architecture: HW + SW

- **Hardware:**
  - Analog: ADC, DAC, PLL, TxRx, RF…etc.
  - Digital: Processor, Interface, Accelerator…etc.
  - Storage: SRAM, DRAM, FLASH, ROM…etc.
- **Software:** OS, Application
A Real Product Example

- Silicon Labs: AeroFONE整合晶片
  - 電源管理單元（PMU）、電池介面和充電電路、數位基頻、類比基頻和四頻RF收發器等主要的手機功能都整合到單晶片CMOS IC中
  - 一舉從典型的BOM表刪去PCB上的200多個插件

Source: EE Times
Multimedia SOC (1/2)

Multimedia SOC (2/2)

系統單晶片的產值佔半導體產業產值的比重將由2004年的19.2%，大幅成長至2008年的23.4%
Top 10 SoC Application Revenue

- **最大的市場: 手機**
  - 低耗電、輕薄短小

<table>
<thead>
<tr>
<th>Application</th>
<th>2005</th>
<th>2008(f)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital Cellular</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage</td>
<td></td>
<td></td>
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<tr>
<td>Consumer Display</td>
<td></td>
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<tr>
<td>Video Game Devices</td>
<td></td>
<td></td>
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<tr>
<td>Computers</td>
<td></td>
<td></td>
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<tr>
<td>Graphics Cards</td>
<td></td>
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<tr>
<td>Digital Audio Player</td>
<td></td>
<td></td>
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<tr>
<td>DVD</td>
<td></td>
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<tr>
<td>Broadband Remote Access</td>
<td></td>
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</tr>
<tr>
<td>WLAN</td>
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</tr>
</tbody>
</table>

資料來源：Dataquest(2005/11)；工研院 IEK-ITIS 計畫整理(2006/03)
VLSI Design Trends

- Design Complexity
  - Transistors
  - Gates
  - RTL
  - SoC

- Design Productivity
  - on-line design
  - place & route
  - Synthesis
  - Reuse
Several conflicting considerations

- **Design complexity**: large number of devices/transistors
- **Cost**: die area, packing, testing, etc.
- **Performance**: optimization requirements for high performance
- **Time-to-market**: about 15% gain for early birds
- **Others**: power, noise, testability, reliability, manufacturability, etc.
Design Challenges (from SIA99)

Current design challenges:
- Complexity (devices & interconnects)
- Noise, power, test
- Copper technology
- SOC methodology
- Timing & function verification

Additional challenges beyond 2005:
- 3D layout
- Signal skew
- Design convergence
- Embedded system
- System test
- Heterogeneous system verification
VLSI Design Flow

1. System Specification
   - Functional / Architecture Design
     - Module declaration:
       ```
       module fz(a,b,c,d,e,Z);
       input a,b,c,d;
       output Z;
       assign Z = ~((a|b&c)|(d&e));
       endmodule
       ```
   - Behavioral representation
   - HDL description
2. Logic Synthesis
   - Logic simulation
   - Circuit analysis
   - Extract & verification
3. Circuit Design
   - Gate-level representation
   - Switch-level representation
VLSI Design Flow

1. Physical Synthesis
2. GDSII files
3. Fabrication
4. Packaging

extract & verification
Logic Synthesis

- Synthesis programs transform HDL descriptions into logic gate networks in a particular library
  - Involve translation and optimization
- Optimization criteria: area, performance, power, and testability
- Logic optimization: technology independent
  - Optimize Boolean expressions but still keep their equivalence
- Technology mapping: technology dependent
  - Map Boolean expressions into a particular cell library
Register Transfer Level Synthesis

Synthesis = Domain Translation + Optimization

---

VHDL

```vhdl
if(A='1') then
  Y<=C + D;
elsif (B='1') then
  Y<=C or D;
else
  Y<=C;
end if
```

Verilog

```verilog
if(A==1)
  Y=C + D;
else if(B==1)
  Y=C | D;
else
  Y=C;
endif
```

---

Domain translation

Optimization (area, timing, power...)

Behavioral domain

Structural domain
Physical Design

- Physical design converts a circuit description into a geometric description (GDSII file)
- Descriptions are used to manufacture a chip
Physical Design Flow

1. Logic partitioning
2. Floorplanning, placement, and pin assignment
3. Routing (global and detailed)
4. Compaction
5. RLC extraction & verification
PowerPC Chip Floorplan

Figure 9-30
A Power PC microprocessor chip with various functional areas delineated. This microprocessor uses the reduced instruction set computing (RISC) architecture. (Photograph courtesy of IBM Corp.)
Silicon Wafers
Wafer and Die

A dice fabricated with other die on the silicon wafer

Enlarged

Wafer diameter is typically 5 to 8 inches.

Nowadays, 12 inches wafer is popular!!
Sawing a Wafer into Chips

Figure 9-33
After testing and sawing, the individual chips are picked up by a robotic arm and placed in the package for die bonding.

(Photograph courtesy of Intel Corp.)
Die and IC with Package

(a) 0.1 inch

(b) silicon die
Packages

Package functions

- Electrical connection of signals and power from chip to board
- Little delay or distortion
- Mechanical connection of chip to board
- Removes heat produced on chip
- Protects chip from mechanical damage
- Compatible with thermal expansion
- Inexpensive to manufacture and test
Chip-to-Package Bonding

Traditionally, chip is surrounded by *pad frame*

- Metal pads on 100 – 200 µm pitch
- Gold *bond wires* attach pads to package
- *Lead frame* distributes signals in package
- Metal *heat spreader* helps with cooling
Package Types

Through-hole vs. surface mount

- 84-pin PLCC
- 14-pin DIP
- 44-pin PLCC
- 387-pin PGA Multichip Module
- 84-pin PGA
- 280-pin QFP
- 86-pin TSOP
- 560-pin BGA
- 40-pin DIP
- 296-pin PGA
Dual In Line Package (DIP)

- DIP --- Dual In Line Package
- DIL --- Dual In Line Package
- PDIP --- Plastic Dual In Line Package
- CDIP --- Ceramic Dual In Line Package
- CerDIP --- Ceramic Dual In Line Package
- MDIP --- Molded Dual In Line Package
- FDIP --- Windowed Frit-Seal Dual In Line Package
- SDIP --- Shrink Dual In Line Package

Plastic J-Leaded Chip Carrier (PLCC) Package

- JLCC --- J-Leaded Chip Carrier
- PLCC --- Plastic J-Leaded Chip Carrier
- CLCC --- Ceramic J-Leaded Chip Carrier

Source: http://www.fpga-guide.com/
Quad Flat Package (QFP)

- QFP --- Quad Flat Pack
- PQFP --- Plastic Quad Flat Pack
- HQFP --- Heat Sink Quad Flat Pack (PQFP with metal plate)
- RQFP --- Plastic Power Quad Flat Pack (similar to HQFP)
- CQFP --- Ceramic Quad Flat Pack
- MQFP --- Metal Quad Flat Pack
- MQFP --- Metric Quad Flat Pack
- BQFP --- Bumpered Quad Flat Pack
- TQFP --- Thin Quad Flat Pack
- VQFP --- Very Thin Quad Flat Pack
- LQFP --- Low Profile Quad Flat Pack
- SQFP --- Shrink Quad Flat Pack (similar to LQFP)

Source: http://www.fpga-guide.com/
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Pin Grid Array (PGA) Package

- PGA --- Pin Grid Array
- PPGA --- Plastic Pin Grid Array
- CPGA --- Ceramic Pin Grid Array

Source: http://www.fpga-guide.com/
Ball Grid Array (BGA) Package

- BGA --- Ball Grid Array
- PBGA --- Plastic Ball Grid Array
- CBGA --- Ceramic Ball Grid Array
- MBGA --- Metal Ball Grid Array
- FBGA --- Fine Pitch Ball Grid Array
- FTBGA --- Fine Pitch Thin Ball Grid Array
- FPBGA --- Fine Pitch Plastic Ball Grid Array
- FCBGA --- Fine Pitch Ceramic Ball Grid Array
- FMBGA --- Fine Pitch Metal Ball Grid Array
- FBGA --- Fine Line Ball Grid Array
- UBGA --- Ultra Fine Line Ball Grid Array
- SBGA --- Super Ball Grid Array
- Flip Chip BGA --- Flip Chip Ball Grid Array
- CSBGA --- Chip Scale Ball Grid Array
- CSP --- Chip Scale Package

Source: http://www.fpga-guide.com/
## Summary

### Table 12.1 Package options

<table>
<thead>
<tr>
<th>Package</th>
<th># I/Os</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual Inline Package (DIP)</td>
<td>8, 14, 16, 20, 28, 40, 64</td>
<td>Two rows of through-hole pins on 100 mil centers. Low cost. Long wires between chip and corner pins.</td>
</tr>
<tr>
<td>Pin Grid Array (PGA)</td>
<td>65–391+</td>
<td>Array of through-hole pins on 100 mil centers. Low thermal resistance and high pin counts.</td>
</tr>
<tr>
<td>Small Outline IC (SOIC)</td>
<td>8,10, 14, 16, 20, 24, 28</td>
<td>Two rows of SMT pins on 50 mil centers. Low cost, good for low-power parts with small pin counts.</td>
</tr>
<tr>
<td>Thin Small Outline Package (TSOP)</td>
<td>28–86+</td>
<td>Two rows of SMT pins on 0.5 or 0.8 mm centers in a thin package. Commonly used for DRAMs.</td>
</tr>
<tr>
<td>Plastic Leadless Chip Carrier (PLCC)</td>
<td>20, 28, 44, 68, 84</td>
<td>J-shaped SMT pins on all four sides on 50 mil centers. Sturdy leads are convenient for socketing.</td>
</tr>
<tr>
<td>Quad Flat Pack (QFP)</td>
<td>44–240</td>
<td>SMT pins on all four sides on 15.7–50 mil centers. High density of I/Os. Available in thin (TQFP) and very thin (VQFP) forms as thin as 1.6 mm.</td>
</tr>
<tr>
<td>Ball Grid Array (BGA)</td>
<td>49–2000+</td>
<td>Array of SMT solder balls on underside of package on 15.7–50 mil centers. Extremely high density of I/Os with low parasitics. Requires specialized assembly and inspection equipment to blindly attach to array of pads on printed circuit board.</td>
</tr>
<tr>
<td>Flip-Chip</td>
<td>Many</td>
<td>Direct connection of chip to printed circuit board through solder balls on top metal layer of chip. Even higher I/O density and lower parasitics than BGA.</td>
</tr>
</tbody>
</table>
IC Fabrication