Devices

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Outlines

- Introduction
  - Ideal I-V Characteristics Transistor
  - C-V Characteristics
  - Nonideal I-V Effect
  - DC Transfer Characteristics
  - Conclusion
CMOS Process
MOS Transistor Symbols

NMOS Enhancement

PMOS Enhancement

NMOS Depletion

NMOS with Bulk Contact

The depletion MOSFET has a physically implanted channel.
MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion

(a) $V_g < 0$

(b) $0 < V_g < V_t$

(c) $V_g > V_t$
Terminal Voltages

- Mode of operation depends on $V_g$, $V_d$, $V_s$
  - $V_{gs} = V_g - V_s$
  - $V_{gd} = V_g - V_d$
  - $V_{ds} = V_d - V_s = V_{gs} - V_{gd}$

- Source and drain are symmetric diffusion terminals
  - By convention, source is terminal at lower voltage
  - Hence $V_{ds} \geq 0$

- nMOS body is grounded. First assume source is 0 too.

- Three regions of operation
  - Cutoff
  - Linear
  - Saturation
nMOS Cutoff

- No channel
- $I_{ds} = 0$
nMOS Linear

- Channel forms
- Current flows from d to s
  - e⁻ from s to d
- $I_{ds}$ increases with $V_{ds}$
- Similar to linear resistor
nMOS Saturation

- Channel pinches off
- $I_{ds}$ independent of $V_{ds}$
- We say current saturates
- Similar to current source

\[ V_{gs} > V_t \]
\[ V_{gd} < V_t \]
\[ V_{ds} > V_{gs} - V_t \]
Outlines

- Introduction
- *Ideal I-V Characteristics Transistor*
- C-V Characteristics
- Nonideal I-V Effect
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Transistor Structure

- n-type transistor:
0.25 micron Transistor (Bell Labs)
I-V Characteristics

- In Linear region, $I_{ds}$ depends on
  - How much charge is in the channel?
  - How fast is the charge moving?
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- \( Q_{\text{channel}} = CV \)
- \( C = C_g = \varepsilon_{ox}WL/t_{ox} = C_{ox}WL \)
- \( V = V_{gc} - V_t = (V_{gs} - V_{ds}/2) - V_t \)

\[ C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]
Carrier Velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
  - $v = \mu E$  \hspace{1cm} $\mu$ called mobility
  - $E = \frac{V_{ds}}{L}$
  - Time for carrier to cross channel:
    - $t = \frac{L}{v}$
nMOS Linear I-V

Now we know

- How much charge $Q_{\text{channel}}$ is in the channel
- How much time $t$ each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

$$= \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

$$\beta = \mu C_{ox} \frac{W}{L}$$
nMOS Saturation I-V

- If \( V_{gd} < V_t \), channel pinches off near drain
  - When \( V_{ds} > V_{dsat} = V_{gs} - V_t \)
- Now drain voltage no longer increases current

\[
I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}
\]

\[
= \frac{\beta}{2} \left( V_{gs} - V_t \right)^2
\]
I-V Curve Characteristics

- **Linear region** \((V_{ds} < V_{gs} - V_{t})\):
  \[I_d = k' \frac{W}{L} \left( (V_{gs} - V_{t})V_{ds} - \frac{1}{2}V_{ds}^2 \right)\]

- **Saturation region** \((V_{ds} \geq V_{gs} - V_{t})\):
  \[I_d = \frac{1}{2} k' \frac{W}{L} (V_{gs} - V_{t})^2\]

- Process transconductance \(k' = \mu C_{ox}\).
- Device transconductance \(\beta = k'W/L\).
Current through a Transistor

From a MOSIS process in 0.5 um process:

- n-type:
  - $k_n' = 73 \mu A/V^2$
  - $V_{tn} = 0.7 V$
- p-type:
  - $k_p' = 21 \mu A/V^2$
  - $V_{tp} = -0.8 V$

Use 0.5 μm parameters. Let $W/L = 3/2$. Measure the current through a minimum-sized n-type transistor at the boundary between linear and saturation regions.

- $V_{gs} = 2V$:
  $$I_d = 0.5k'(W/L)(V_{gs}-V_t)^2 = 0.5 \times 73 \times (3/2) (2-0.7)^2 = 93 \mu A$$
- $V_{gs} = 5V$:
  $$I_d = 0.5k'(W/L)(V_{gs}-V_t)^2 = 0.5 \times 73 \times (3/2) (5-0.7)^2 = 1 mA$$
pMOS I-V

- All dopings and voltages are inverted for pMOS
- Mobility $\mu_p$ is determined by holes
  - Typically 2-3x lower than that of electrons $\mu_n$
  - 120 cm$^2$/V*s in AMI 0.6 $\mu$m process
- Thus pMOS must be wider to provide same current
  - In this class, assume $\mu_n / \mu_p = 2$

- *** plot I-V here
## Summary of Operation Regions

### Table 2.2  Relationships between voltages for the three regions of operation of a CMOS inverter

<table>
<thead>
<tr>
<th></th>
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<th>Linear</th>
<th>Saturated</th>
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- **C-V Characteristics**
- Nonideal I-V Effect
- DC Transfer Characteristics
- Conclusion
Capacitance

- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion
MOSFET Gate as Capacitor

- Basic gate structure with the parallel-plate capacitor
- Formula for parallel plate capacitance:
  \[ C_g = C_{ox} \cdot WL \], where \( C_{ox} = \varepsilon_{ox} / t_{ox} \)
- Permittivity of silicon:
  \( \varepsilon_{ox} = 3.46 \times 10^{-13} \, \text{F/cm} \)
Transistor Gate Parasitics (1/2)

- Gate capacitance consists of two components:
  1) Intrinsic capacitance.
  2) Overlapped capacitance

- Intrinsic capacitance:

<table>
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<th>Table 2.1</th>
<th>Approximation of intrinsic MOS gate capacitance</th>
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<td>$C_0$</td>
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</tr>
<tr>
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<td>0</td>
</tr>
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Gate-source/drain overlap capacitance Intrinsic capacitance:

- $C_{gs\text{ (overlap)}} = C_{gsol} W$
- $C_{gd\text{ (overlap)}} = C_{gdol} W$

**FIG 2.10** Overlap capacitance
Diffusion Wire Capacitance (1/3)

Capacitances formed by p-n junctions:

- \( C_{sb} = A_S x C_{jbs} + P_S x C_{jbssw} \)
- \( C_{db} = A_D x C_{jbd} + P_D x C_{jbdsw} \)

Diagram of a diffusion wire with annotations for substrate capacitance, bottomwall capacitance, and sidewall capacitances.
Diffusion Wire Capacitance (2/3)

- Sidewall and bottomwall capacitance can be calculated from the junction capacitance depending on the function of voltage across junction:
  - \( C_j(V_r) = \frac{C_{j0}}{\sqrt{1 + V_r/V_{bi}}} \)
- Zero-bias depletion capacitance:
  - \( C_{j0} = \frac{\varepsilon_{si}}{t_d} \)
- Depletion region width:
  - \( t_{d0} = \sqrt{(1/N_A + 1/N_D)2\varepsilon_{si} V_{bi}/q} \)
Diffusion Wire Capacitance (3/3)

- Undesirable, called *parasitic* capacitance

- Capacitance depends on area and perimeter
  - Use smaller and fewer diffusion nodes
  - Comparable to $C_g$ for contacted diff
  - $\frac{1}{2} C_g$ for uncontacted node
  - Varies with process
Poly/Metal Wire Capacitance

Two components:
- Parallel plate to Substrate
- Fringe to Substrate
Metal Coupling Capacitances

Coupling to adjacent wires on same layer or wires on above/below layers:
Example: Parasitic Capacitance Measurement

- **n-diffusion capacitance:**
  - Bottomwall = \((3 \times 0.75 + 1 \times 1) \times 0.6 = 1.95 \text{ fF}\).
  - Sidewall = \((0.75 + 3 + 0.25 + 1 + 1 + 4) \times 0.2 = 2 \text{ fF}\).

- **Metal capacitance:**
  - Parallel plate = 0.15 fF.
  - Fringe = 0.72 fF.

**N-diffusion:**
- Bottomwall capacitance: 0.6 fF/\mu m
- Sidewall capacitance: 0.2 fF/\mu m

**Metal 1:**
- Plate: 0.04 fF/\mu m
- Fringe: 0.09 fF/\mu m
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Channel Length Modulation (1/2)

\[ V_{ds} < V_{gs} - V_t \]

\[ V_{ds} = V_{gs} - V_t \]

\[ V_{ds} > V_{gs} - V_t \]

\[ L_{eff} = L - L_d \text{ due to reverse bias between drain and body (i.e., } V_{db} = V_{ds} \)
Modified drain current equation with channel length effect:

\[ I_{D,\text{sat}} = \frac{1}{2} k' \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \]

\( \lambda \) factor describes small dependence of drain current on \( V_{ds} \) at saturation.

\( \lambda \) factor is measured empirically.

Equation has a discontinuity between linear and saturation regions --- small enough to be ignored.

Channel length is very important to analog design because it reduces the gain of amplifier.
Threshold Voltage, $V_t$ (1/2)

$$V_t = V_{fb} + \phi_s + \frac{Q_b}{C_{ox}} + V_{II} = V_{t0} + \gamma \left( \sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right) = V_{t0} + \Delta V_t$$

$$\phi_s = 2|\phi_F| = 2 \frac{kT}{q} \ln \frac{N_a}{n_i} \quad \gamma = \frac{\sqrt{2q \varepsilon_{si} N_a}}{C_{ox}}$$

- $V_{fb} = \text{Flatband voltage}$; depends on difference in work function between gate and substrate and on fixed surface charge
- $\phi_s = \text{Surface potential}$ (about $2\phi_F$), where $\phi_F$ is Fermi potential.
- $Q_b = \text{Value of charge across the parallel plate capacitor.}$
Threshold Voltage, $V_t$ (2/2)

- $V_{\|} = $ Voltage adjustment.
- $V_{t0} = $ Threshold Voltage without Body effect.

**Body effect**

- **Definition:** Variation of threshold voltage with source/substrate voltage is called as.
- **Reorganize threshold voltage equation:**
  \[ V_t = V_{t0} + \Delta V_t \]

- Threshold voltage is a function of source/substrate voltage $V_{sb}$.
- Body effect factor $\gamma$ is the coefficient for the $V_{sb}$ dependence factor.
Example: Threshold Voltage

\[ V_t = V_{fb} + \phi_s + \frac{Q_{b0}}{C_{ox}} + V_{II} = -0.91 + 0.58 + \frac{1.4 \times 10^{-8}}{1.73 \times 10^{-7}} + 0.92 \]

= 0.68 V

\[ \gamma = \frac{\sqrt{2q\varepsilon_{si}N_a}}{C_{ox}} = \frac{\sqrt{2 \times (1.6 \times 10^{-19}) \times (1.0 \times 10^{-12}) \times 10^{15}}}{1.73 \times 10^{-7}} = 0.1 \]

Let \( V_{sb} = 5 \) V

\[ \Delta V_t = \gamma \left( \sqrt{\phi_s} + V_{sb} - \sqrt{\phi_s} \right) = 0.1 \left( \sqrt{0.58} + 5 - \sqrt{0.58} \right) = 0.16 \]
Leakage Currents

- A variety of leakage currents draw current away from the main logic path.
- The **subthreshold current** is one particularly important type of leakage current.

Sources of leakage current:
- Subthreshold current (a.k.a. Weak inversion current): Transistors can’t abruptly turn ON or OFF
- Drain-induced barrier lowering
- Reverse-biased p-n junctions: Reverse-biased PN junction diode current
- Gate oxide tunneling: Tunneling through ultra thin gate dielectric
- Hot carriers
- Punchthrough currents
Subthreshold Current

Subthreshold current:

- \( I_{\text{sub}} = k e^{\left(\frac{(V_{\text{gs}} - V_t)}{S \ln 10}\right)} [1 - e^{-q V_{ds}/kT}] \)
- Subthreshold current is an exponential function of gate voltage.
- Subthreshold current is a function of \( V_t \).
- Adjust \( V_t \) by changing the substrate bias to control leakage.

Subthreshold slope \( S \) characterizes weak inversion current.
DIBL

Drain-Induced Barrier Lowering

- Drain voltage also affects $V_t$

$$V'_t = V_t - \eta V_{ds}$$

- High drain voltage causes subthreshold leakage to increase.
Reverse-Biased PN Junction Leakage

- Reverse-biased p-n junctions have some leakage

$$I_D = I_S \left( e^{\frac{V_D}{kT}} - 1 \right)$$

- $I_S$ depends on doping levels
  - And area and perimeter of diffusion regions
  - Typically < 1 fA/µm²
Gate Oxide Tunneling Leakage

- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current (from [Song01])
- Negligible for older processes
- May soon be critically important in modern process

![Graph showing gate oxide tunneling leakage current versus V_DD for different tox thicknesses.]

\[ J_G (A/cm^2) \]

\[ 10^{-9} \]

\[ 10^{-6} \]

\[ 10^{-3} \]

\[ 10^0 \]

\[ 10^3 \]

\[ 10^6 \]

\[ 10^9 \]

\[ V_{DD} \text{ trend} \]
Hot Carriers

Electric fields across channel impart high energies to some carriers

- These “hot” carriers may be blasted into the gate oxide where they become trapped
- Accumulation of charge in oxide causes shift in $V_t$ over time
- Eventually $V_t$ shifts too far for devices to operate correctly

Choose $V_{DD}$ to achieve reasonable product lifetime

- Worst problems for inverters and NORs with slow input risetime and long propagation delays
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Activity

1) If the width of a transistor increases, the current will
   increase  decrease  not change

2) If the length of a transistor increases, the current will
   increase  decrease  not change

3) If the supply voltage of a chip increases, the maximum
   transistor current will
   increase  decrease  not change

4) If the width of a transistor increases, its gate capacitance will
   increase  decrease  not change

5) If the length of a transistor increases, its gate capacitance will
   increase  decrease  not change

6) If the supply voltage of a chip increases, the gate capacitance
   of each transistor will
   increase  decrease  not change
Activity

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DC Response

**DC Response: \( V_{\text{out}} \) vs. \( V_{\text{in}} \) for a gate**

**Ex: Inverter**
- When \( V_{\text{in}} = 0 \) \( \rightarrow \) \( V_{\text{out}} = V_{\text{DD}} \)
- When \( V_{\text{in}} = V_{\text{DD}} \) \( \rightarrow \) \( V_{\text{out}} = 0 \)
- In between, \( V_{\text{out}} \) depends on transistor size and current
- By KCL, must settle such that \( I_{\text{dsn}} = |I_{\text{dsp}}| \)
- We could solve equations
- But graphical solution gives more insight
Transistor Operation

- Current depends on region of transistor behavior
- For what $V_{\text{in}}$ and $V_{\text{out}}$ are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?
# nMOS Operation

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**Diagram:**

- $V_{DD}$
- $V_{in}$
- $I_{dsp}$
- $I_{dsn}$
- $V_{out}$
nMOS Operation

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![nMOS Operation Diagram](image-url)
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$V_{gsn} = V_{in}$

$V_{dsn} = V_{out}$
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$V_{gsn} = V_{in}$

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# pMOS Operation

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![pMOS Circuit Diagram](image)

The diagram shows a pMOS transistor with inputs $V_{in}$ and $V_{DD}$, output $V_{out}$, and currents $I_{dsp}$ and $I_{dsn}$. The expressions for the different regions of operation are as follows:

- **Cutoff**: $V_{gsp} > V_{gsp} < V_{dsp} > V_{dsp} <$
- **Linear**: $V_{gsp} <$
- **Saturated**: $V_{gsp} <$
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\[
V_{gsp} = V_{in} - V_{DD} \quad V_{tp} < 0
\]

\[
V_{dsp} = V_{out} - V_{DD}
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</tr>
<tr>
<td>$V_{in} &gt; V_{DD} + V_{tp}$</td>
<td>$V_{in} &lt; V_{DD} + V_{tp}$</td>
<td>$V_{in} &lt; V_{DD} + V_{tp}$</td>
</tr>
<tr>
<td>$V_{dsp} &gt; V_{gsp} - V_{tp}$</td>
<td>$V_{dsp} &lt; V_{gsp} - V_{tp}$</td>
<td>$V_{dsp} &lt; V_{gsp} - V_{tp}$</td>
</tr>
<tr>
<td>$V_{out} &gt; V_{in} - V_{tp}$</td>
<td>$V_{out} &lt; V_{in} - V_{tp}$</td>
<td>$V_{out} &lt; V_{in} - V_{tp}$</td>
</tr>
</tbody>
</table>

$V_{gsp} = V_{in} - V_{DD}$

$V_{tp} < 0$

$V_{dsp} = V_{out} - V_{DD}$
I-V Characteristics

Make pMOS is wider than nMOS such that $\beta_n = \beta_p$
Current vs. $V_{out}$, $V_{in}$
Load Line Analysis

For a given $V_{in}$:
- Plot $I_{dsn}$, $I_{dsp}$ vs. $V_{out}$
- $V_{out}$ must be where $|currents|$ are equal in

![Graph showing load line analysis with $V_{in}$, $I_{dsn}$, $I_{dsp}$, $V_{out}$, and $V_{DD}$]
Load Line Analysis

\[ V_{\text{in}} = 0 \]

\[ V_{\text{in0}} \]

\[ I_{\text{dsn}}, |I_{\text{dsp}}| \]

\[ V_{\text{out}} \rightarrow V_{\DD} \]

\[ V_{\text{in0}} \]
\[ V_{in} = 0.2V_{DD} \]
Load Line Analysis

\[ V_{in} = 0.4V_{DD} \]
Load Line Analysis

\[ V_{in} = 0.6V_{DD} \]
Load Line Analysis

\[ V_{in} = 0.8V_{DD} \]
Load Line Analysis

\[ V_{in} = V_{DD} \]

\[ I_{dsn}, |I_{dsp}| \]

\[ V_{in0}, V_{in1}, V_{in2}, V_{in3}, V_{in4}, V_{in5} \]

\[ V_{out}, V_{DD} \]
Load Line Summary

\[ V_{\text{in0}} \rightarrow V_{\text{in1}} \rightarrow V_{\text{in2}} \rightarrow V_{\text{in3}} \rightarrow V_{\text{in4}} \rightarrow V_{\text{out}} \]

\[ |I_{\text{dsn}}| \rightarrow |I_{\text{dsp}}| \rightarrow V_{\text{DD}} \]
DC Transfer Curve

- Transcribe points onto $V_{in}$ vs. $V_{out}$ plot
Operating Regions

Revisit transistor operating regions

<table>
<thead>
<tr>
<th>Region</th>
<th>nMOS</th>
<th>pMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
</tr>
<tr>
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Operating Regions

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<td>Linear</td>
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<td>Saturation</td>
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<tr>
<td>E</td>
<td>Linear</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>

\[ V_{\text{out}} \]

\[ V_{\text{in}} \]
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed* gate
- Other gates: collapse into equivalent inverter
Logic Levels

- **Solid logic 0/1** defined by $V_{SS}/V_{DD}$.
- Inner bounds of logic values $V_L/V_H$ are directly determined by circuit properties, as in some other logic families.
- Levels at output of one gate must be sufficient to drive next gate.

<table>
<thead>
<tr>
<th>$V_{DD}$</th>
<th>logic 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_H$</td>
<td>unknown</td>
</tr>
<tr>
<td>$V_L$</td>
<td></td>
</tr>
<tr>
<td>$V_{SS}$</td>
<td>logic 0</td>
</tr>
</tbody>
</table>
Inverter Transfer Curve (1/3)

- Transfer curve shows static input/output relationship — hold input voltage, measure output voltage.

Nonlinear!
Inverter Transfer Curve (2/3)

\[ V_{OL} < V_{IL} \]

\[ V_{OH} > V_{IH} \]

- \( V_{IL} = 1.2V \)
- \( V_{OH} = 4.8V \)
- \( V_{IH} = 2.2V \)
- \( V_{OL} = 0.4V \)
Choose threshold voltages at points where slope of transfer curve = -1.

Inverter has a high gain between \( V_{IL} \) and \( V_{IH} \) points, low gain at outer regions of the transfer curve.

Note that logic 0 and 1 regions are not equal sized—in this case, high pull-up resistance leads to smaller valid logic 1 range.
Noise Margins

How much noise can a gate input see before it does not recognize the input?

\[ \text{NM}_H = V_{OH} - V_{IH} \]
\[ \text{NM}_L = V_{IL} - V_{OL} \]
Logic Levels

To maximize noise margins, select logic levels at

\[ V_{\text{in}} \rightarrow V_{\text{out}} \]

\[ V_{\text{DD}} \]

\[ \beta_p / \beta_n > 1 \]
Logic Levels

To maximize noise margins, select logic levels at
- unity gain point of DC transfer characteristic

\[ V_{DD}, V_{OH}, V_{OL} \]

\[ V_{in}, V_{out}, V_{IL}, V_{IH}, V_{DD}, V_{OL}, V_{OH} \]

Unity Gain Points
Slope = -1

\[ \beta_p / \beta_n > 1 \]

Schematic diagram with symbols and annotations.
Conclusion

Widely discuss the following items:

- I-V Characteristics Transistor
- C-V Characteristics
- Nonideal I-V Effect
- DC Transfer Characteristics